Claims

What is claimed is:

1. A memory device, comprising:

a circuit device defining a horizontal surface and a non-horizontal surface; and

a porous oxide over said circuit device, said porous oxide having a first thickness extending perpendicularly from said horizontal surface and a second thickness extending generally perpendicularly from said non-horizontal surface, wherein said second thickness is different from said first thickness.

2. The memory device in claim 1, wherein said porous oxide comprises an oxide defining at least one pore.

3. The memory device in claim 2, wherein said porous oxide comprises a plurality of silicon atoms and a plurality of oxygen atoms, wherein said plurality of silicon atoms and said plurality of oxygen atoms define a lattice constant; and wherein at least one dimension of said at least one pore is greater than said lattice constant.

4. The memory device in claim 3, wherein said dimension of said at least one pore is at least 10 angstroms.

5. The memory device in claim 4, wherein said dimension of said at least one pore ranges from 10 to 20 angstroms.

6. The memory device in claim 4, further comprising a dopant in at least one pore.

7. The memory device in claim 6, wherein said dopant consists of a selection from boron, carbon, phosphorous, fluorine, nitrogen, and combinations thereof.

8. A portion of a semiconductor device, comprising:

a support surface defining at least two elevations within said semiconductor device; and

a doped insulator non-conformally over said support surface, wherein said insulator is thinner between two consecutive elevations of said support surface than said insulator directly over at least one of said consecutive elevations.

9. The portion of a semiconductor device in claim 8, wherein said doped insulator is non-continuously over said support surface.

10. The portion of a semiconductor device in claim 8, wherein said doped insulator is a boron-doped insulator.

11. The portion of a semiconductor device in claim 8, wherein said doped insulator is a doped oxide.

12. The portion of a semiconductor device in claim 8, further comprising an undoped insulator between said doped insulator and said support surface.

13. The portion of a semiconductor device in claim 12, wherein said undoped insulator is non-conformally over said support surface.

14. A material for a semiconductor device, comprising a boron-doped oxide on at least one horizontal portion of said semiconductor device more so than on a vertical portion of said device.

15. The material in claim 14, wherein said semiconductor device includes a layer defining a trench; wherein said at least one horizontal portion comprises a bottom of said trench; and wherein said vertical portion is a sidewall of said trench.

16. The material in claim 15, wherein said at least one horizontal portion further comprises a surface of said layer even with a top of said trench.

17. A method of processing an in-process semiconductor device, comprising:
non-conformally depositing an oxide over said in-process semiconductor device;
doping said oxide; and
depositing an insulator over said oxide.

18. The method in claim 17, further comprising:
initiating a removal of at least a portion of said insulator; and
halting said removal using said oxide.

19. The method in claim 18, wherein said initiating step comprises initiating an etching of said insulator; and wherein said halting step comprises using said oxide as an etch stop.

20. The method in claim 18, wherein said initiating step comprises initiating a planarization of said insulator.

21. The method in claim 20, wherein said step of initiating a planarization of said insulator comprises initiating a chemical-mechanical planarization of said insulator; and wherein said halting step comprises using said oxide as a CMP stop.

22. A method of providing oxide for an in-process semiconductor device, comprising:
depositing a first oxide over said in-process semiconductor device; and
non-conformally depositing a porous second oxide onto said first oxide.

23. The method in claim 22, wherein said step of depositing a first oxide comprises depositing said first oxide in a chamber; and wherein said step of non-conformally

depositing a porous second oxide comprises depositing said second oxide in said chamber.

24. The method in claim 22, wherein said step of non-conformally depositing a porous second oxide comprises reacting methylsilane with hydrogen peroxide.

25. The method in claim 22, wherein said step of non-conformally depositing a porous second oxide comprises reacting H_3SiCH_3 with H_2O_2.

26. The method in claim 25, wherein said step of non-conformally depositing a porous second oxide further comprises:

cooling said in-process semiconductor device to about 0°C before said reacting step; and

providing a temperature of about 450°C inside said chamber after said reacting step.

27. The method in claim 26, wherein said step of depositing a first oxide comprises reacting silane with hydrogen peroxide.

28. A method of providing a doped oxide, comprising:

flowing an oxide precursor over a portion of a semiconductor device;

forming an oxide from said precursor; and

subsequently annealing said oxide in an atmosphere containing a dopant.

29. The method in claim 28, wherein said annealing step comprises annealing said oxide in an atmosphere consisting of a selection of PH_3, a phosphate, a phosphite, NF_3, F_2, C_2H_6, trimethyl silane, CH_4, NH_3, B_2H_6, and combinations thereof.

30. The method in claim 29, wherein said annealing step further comprises annealing at a temperature ranging from 400 to 800°C, at a pressure ranging from 0.5 to 760 Torr, and for a time ranging from 10 seconds to 5 minutes.

31. A method of processing a surface of an in-process memory device, comprising:

providing said surface as part of said memory device using a non-CVD process;

flowing a material onto said surface;

turning said material into a first oxide; and

doping said first oxide.

32. The method in claim 31, wherein said step of providing said surface comprises providing a barrier oxide using a Flowfill process; and wherein said method further comprises blocking diffusion of a dopant from said first oxide using said barrier oxide.

33. The method in claim 32, wherein said step of doping said first oxide comprises:

doping a first portion of said first oxide with a first impurity; and

doping a second portion of said first oxide with a second impurity.

34. A method of providing an etch stop for a semiconductor device, comprising:

providing at least one support surface as part of said semiconductor device, said surface having a horizontal portion and a non-horizontal portion;

depositing an oxide onto said support surface, wherein said oxide has a uniform thickness on said horizontal portion and a variable thickness on said non-horizontal portion; and

doping said oxide.

35. The method in claim 34, wherein said depositing step comprises depositing said oxide by way of a CVD process.

36. The method in claim 35, wherein said depositing step comprises depositing said oxide by way of an HDP CVD process.

37. A method of providing a CMP stop for a semiconductor device, comprising:

providing an element of said semiconductor device, said element having a top and a side;

depositing an oxide over said element, wherein said depositing leaves more of said oxide on said top than on said side; and

annealing said oxide in a doping atmosphere.

38. The method in claim 37, wherein said step of depositing an oxide comprises:

flowing a precursor to said oxide over said element; and

heating said precursor.

39. The method of claim 38, wherein said step of depositing an oxide comprises depositing said oxide using a spin-on-glass process.

40. A method of selectively doping a circuit device material, comprising:

depositing an oxide over a first horizontal surface of said circuit device material to the exclusion of a vertical surface of said material;

introducing a dopant into said oxide; and

diffusing said dopant from said oxide into said material.

41. The method in claim 40, further comprising a step of depositing a diffusion barrier over a second horizontal surface of said material; and wherein said step of depositing an oxide further comprises depositing said oxide over said diffusion barrier.

42. A method of filling a trench included as part of a semiconductor device, comprising:

reacting methylsilane with hydrogen peroxide in a chamber containing said semiconductor device;

allowing a product from a reaction of said methylsilane and said hydrogen peroxide to at least fill said trench;

changing said product into a silicon oxide; and

heating said silicon oxide in a boron atmosphere.

43. A fabrication process for a DRAM including a semiconductor substrate, said process comprising:

depositing an undoped self-planarizing first oxide over an in-process device included as a part of said DRAM;

depositing an undoped self-planarizing second oxide over said first oxide; and

doping said second oxide.

44. The process in claim 43, further comprising:

depositing an insulation layer over said second oxide;

planarizing said insulation layer; and

using said second oxide as a planarization stop.

45. The process in claim 43, further comprising:

depositing an insulation layer over said second oxide;

etching an opening in said insulation layer; and

using said second oxide as an etch stop.

46. The process in claim 45, wherein said step of using said second oxide as an etch stop comprises using a portion of said second oxide over said substrate as said etch stop.

47. The process in claim 46, said step of etching an opening in said insulation layer comprises etching said insulation layer at a first etch rate; and wherein said step of using said second oxide as an etch stop comprises etching said second oxide at a second etch rate, wherein said second etch rate is less than said first etch rate.

48. The process in claim 47, wherein said step of etching said insulation layer comprises exposing said insulation to a selection of an HF vapor and an HF liquid.

49. The process in claim 48, wherein said step of etching said insulation layer comprises exposing said insulation to a buffered HF liquid having a temperature of about 23°C.

50. The process in claim 48, wherein said step of etching said second oxide comprises exposing said second oxide to said selection.

51. A damascene process, comprising:

providing a material over a semiconductor substrate, said material having a fluid property;

forming an oxide from said material in response to allowing said material to lose said fluid property;

providing an insulation layer over said oxide;

etching an opening in said insulation layer;

halting said etching with said oxide; and

depositing a conductive material within said opening.

52. The damascene process in claim 51, further comprising a step of removing at least a portion of said oxide after said halting step and before said depositing step.

53. The damascene process in claim 52, wherein said step of forming an oxide comprises:

forming said oxide onto a BPSG layer; and

doping said oxide before said step of providing an insulation layer.

54. The damascene process in claim 52, wherein:

said step of providing a material comprises depositing said material having a planar surface and defining at least two different thicknesses, wherein depositing said material occurs before providing said insulation layer; and

said method further comprises doping said oxide before providing said insulation layer.

55. ~~The~~ damascene process in 54, wherein said step of depositing said material comprises depositing said material over a gate and over a conductive plug next to said gate, wherein a top of said plug is lower in elevation than a top of said gate.

56. The damascene process in claim 55, wherein said etching step comprises etching using a selection of a reactive sputter process and a plasma process.

57. The damascene process in claim 56, wherein said etching step comprises plasma etching using a gas comprising fluorine, wherein said gas includes a selection of CHF_3, CF_4, and C_2F_6.

58. The damascene process in claim 57, wherein said plasma etching step comprises:

providing a chamber configured to accommodate said semiconductor substrate;

flowing CF_4 into said chamber at a rate of 50 sccm;

flowing CHF_3 into said chamber at a rate of 50 sccm;

flowing Argon into said chamber at a rate of 1000 sccm;

providing pressure of 0.2 to 0.002 Torr inside said chamber; and

providing 750 W of RF power to said chamber.

59. A method of forming oxide over a transistor gate and over a substrate extending laterally from under said gate, said method comprising:

forming an undoped first oxide over said gate and said substrate;

forming an undoped second oxide over said first oxide;

doping said second oxide after forming said second oxide;

depositing insulation over said second oxide after doping said second oxide;

initiating a removal of a portion of said insulation; and

stopping said removal with said second oxide.

60. ~~The~~ method in claim 59, wherein said step of forming an undoped first oxide comprises forming a TEOS-based oxide.

61. The method in claim 59, wherein said step of forming an undoped first oxide comprises forming a continuous silicon dioxide layer.

62. The method in claim 59, wherein said step of forming an undoped first oxide comprises forming a first oxide that is thicker over said gate than lateral to said gate, and wherein said first oxide is thicker over said substrate than lateral to said gate.

63. The method in claim 62, wherein said step of forming an undoped first oxide comprises forming a non-porous first oxide.

64. The method in claim 62, wherein said step of forming an undoped second oxide comprises forming a second oxide that is thicker over said gate than lateral to said gate, and wherein said second oxide is thicker over said substrate than lateral to said gate.

65. The method of claim 64, wherein said step of forming an undoped second oxide comprises:

depositing 500 to 1000 Angstroms of said second oxide over said gate;

depositing 500 to 1000 Angstroms of said second oxide over said substrate; and

depositing 0 to 50 Angstroms of said second oxide lateral to said gate.

66. A method of depositing an interlayer dielectric, comprising:

providing a first level of a semiconductor device, said first level defining a topography and comprising insulation;

depositing BSG onto discrete portions of said topography, said BSG having a dielectric constant of at most 3; and

providing a second level of said semiconductor device over said BSG.

67. The method in claim 66, wherein said step of depositing BSG comprises:

depositing glass onto said topography, said depositing resulting in a planar surface of said glass; and

lowering a dielectric constant of said glass.

68. The method in claim 67, wherein said step of depositing glass comprises:

flowing a silicon oxide precursor over said topography; and

hardening said precursor into a silicon oxide.

69. The method in claim 68, wherein said step of lowering a dielectric constant of said glass comprises doping said silicon oxide with boron.

70. The method in claim 69, wherein said step of providing a first level of a semiconductor device comprises providing a first level further comprising at least one conductive structure.

71. A method of processing a portion of a device including a higher horizontal surface, a lower horizontal surface, and a non-horizontal surface, said method comprising:

providing an oxide in a non-conformal manner over said higher horizontal surface, said lower horizontal surface, and said non-horizontal surface; and

introducing an impurity into said oxide.

72. The method in claim 71, wherein said step of providing an oxide in a non-conformal manner comprises providing an oxide having a first thickness on said higher horizontal surface, a second thickness on said lower horizontal surface, and a third thickness on said non-horizontal surface, wherein said first, second, and third thicknesses are different.

73. The method in claim 72, wherein said step of providing an oxide comprises providing an oxide having a first thickness greater than said second thickness.

74. The method in claim 72, wherein said step of providing an oxide comprises providing an oxide having a second thickness greater than said first thickness.

75. The method in claim 74, wherein said step of providing an oxide in a non-conformal manner comprises reacting methylsilane and hydrogen peroxide in an environment including a substrate having a temperature of about 20°C.

76. The method in claim 75, wherein said step of providing an oxide comprises providing an oxide over a non-horizontal surface connecting said higher horizontal surface to said lower horizontal surface.

77. A method of forming a doped oxide over a substrate, comprising:

reacting a methylsilane with hydrogen peroxide proximate said substrate;

forming an oxide from a product of said methylsilane and said hydrogen peroxide; and

introducing a dopant into said oxide.

78. The method in claim 77, wherein said reacting step comprises reacting said hydrogen peroxide with a selection comprising dimethylsilane, trimethylsilane, tetramethylsilane, pentamethyldisilane, and combinations thereof.

79. A semiconductor device, comprising:

a first portion of doped porous oxide on a first surface of said semiconductor device, wherein said first portion of doped oxide has a first thickness; and

a second portion of doped porous oxide on a second surface of said semiconductor device, wherein said second portion has a second thickness different from said first thickness.

80. The device in claim 79, wherein said first surface defines a first plane at a first elevation, and wherein said second surface defines a second plane at a second elevation.

81. The device in claim 80, wherein said first surface defines a first horizontal surface, and wherein said second surface defines a second horizontal surface.

82. The device in claim 81, further comprising a third portion of doped porous oxide on a third surface of said semiconductor device, wherein said third portion has a third thickness different from said first and second thickness.

83. The device in claim 83, wherein said third surface defines a transition from said first surface to said second surface.

84. A material for a portion of a semiconductor device, wherein said portion defines a varying topography, said material comprising a boron-doped porous oxide having varying thicknesses over said portion.

85. The material in claim 84, wherein said oxide is thicker at a higher elevation of said portion than at a lower elevation of said portion.

86. The material in claim 85, wherein said oxide is thicker at a horizontal section of said portion than at a non-horizontal section of said portion.

87. The material in claim 86, wherein said oxide has a thickness of zero at at least a part of said non-horizontal section.

88. The material in claim 87, wherein said oxide has a thickness of zero at said lower elevation.